Fundamentals of Gate Drivers

Power Flow Systems

Abstract:

In high power applications, because of the low current capabilities of output of a logic IC (PWM controller), charging the gate capacitance would require an excessive amount of time, most likely longer than the duration of a switching period. Hence dedicated drivers must be used to apply a voltage and provide drive current to the gate of the power device. This can be a driver circuit and it may be implemented as dedicated ICs, discrete transistors or transformers. It can also be integrated within a PWM controller IC.

A gate driver is a power amplifier that takes a low-power input from a controller IC and generates the necessary high-current gate drive for a power device. It is typically used when a PWM controller is unable to provide sufficient output current to charge and discharge the gate capacitance of the associated power device effectively. Gate drivers play a crucial role in ensuring fast and efficient switching of MOSFETs, IGBTs, or other power transistors.

1. Types of gate drivers:

In a leg configuration, gate drivers can be categorized based on the side of the transistor which they are needed for:

1.1. Low-Side Drivers:

These are used to drive the gate of a transistor whose source (in the case of MOSFETs) or emitter (in the case of IGBTs) is connected to ground or a common reference point. Low-side drivers are simpler since the gate is referenced to a fixed voltage.

1.2. High-Side Drivers:

These are used for transistors where the source or emitter is connected to a voltage that floats relative to ground. High-side drivers require more complex circuitry, such as level shifters or bootstrap circuits, to provide the necessary gate voltage referenced to the floating source/emitter.

1.3. High-side/Low-Side Drivers:

These are specialized gate drivers designed to control both high-side and low-side power transistors (MOSFETs or IGBTs) in circuits such as half-bridge, full-bridge, or push-pull topologies. These drivers are commonly used in applications like motor control, DC-DC converters, and inverters. They ensure proper switching of both high-side and low-side transistors while maintaining high efficiency and avoiding issues like shoot-through.

2. Required Gate Current:

Fig.1 shows the Ig and Vgs waveforms during MOSFET turn on and turn off intervals. Each steps are described with more details here.

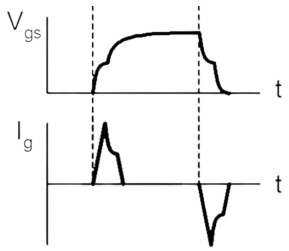

Fig.1. Ig and Vgs waveform during turn on and turn off intervals of the MOSFET

To select the optimal gate driver IC for our application, accurate calculation of the required current is essential. There are two methods to determine the required gate current. As shown in Fig. 2, it is assumed that the gate current (Ig) is a pulse, and the goal is to calculate the peak value of this pulse, I_G.

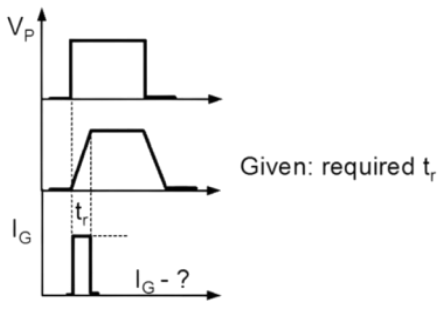

Fig.2. simplified Ig waveform to calculate the required current capability of the gate driver

2.1. Method 1: Equivalent Capacitor:

In this method, the equivalent capacitor is utilized to determine the amount of current required to be supplied to the gate in order to switch the transistor on and off within a specified time frame.

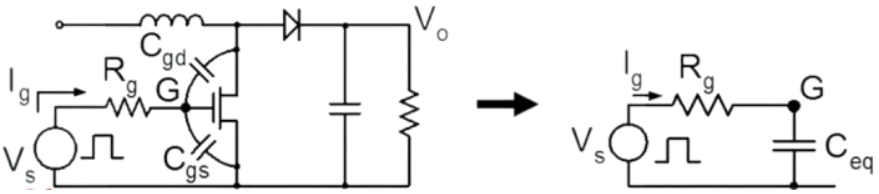

Fig.3. equivalent capacitor to calculate the required Ig

The equivalent capacitance (C_{eq}) represents the total capacitance that needs to be charged or discharged in order to turn the transistor on or off. It combines the effects of all relevant capacitances in the circuit and helps to determine the current required for the switching process.

$$Q_{total} = V_{GS}.C_{GS} + C_{GD}.(V_{GS} + V_O) \quad (1)$$

$$C_{eq} = \frac{Q_{total}}{V_{GSmax}} = C_{GS} + C_{GD}.(1 + \frac{V_o}{V_{GSmax}})$$

Where $\frac{V_o}{V_{GSmax}}$ is the miller effect and it occurs at step 3 in the turn–on process and step 2 in the turn–off process. Check here for more details. To calculate the required constant gate current (I_G):

$$Q_{total} = I_G.t_r = C_{eq}.V_{GSmax} \quad (2)$$

$$I_G = \frac{C_{eq}.V_{GSmax}}{t_r}$$

2.2. Method 2: Gate Input Charge

In this method, the Q_{total} from data sheet can be used to calculate I_G. The curve in data sheet looks like Fig.4.

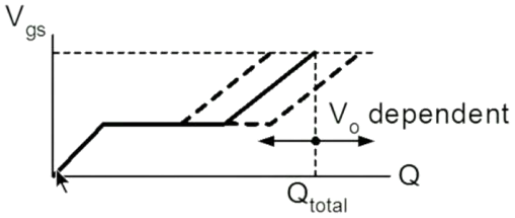

Fig.4. Q_{total} value in data sheet

To calculate the I_G value, following equation can be used:

$$I_G = \frac{Q_{total}}{t_r} \quad (3)$$

According to method 1, the I_G value depends on V_o, C_{GD} and C_{GS} and according to method 2, I_G depends on I_D, V_o, C_{GD} and C_{GS}.

3. Loss:

The switching action in the MOSFET transistor in power applications results in some unavoidable losses one of which is the gate driver loss. Turning on and off the MOSFET involves charging and discharging the C_{ISS} capacitor respectively. To change the voltage across a capacitor, a certain amount of charge has to be transferred. The amount of charge required to change the gate voltage between 0 V and V_{GSmax} (supply of the gate driver), is characterized by the typical gate charge vs. gate–to–source voltage curve as shown in Fig.4.

During the turn on, the C_{eq} needs to be charged up to V_{GS}. In every switching cycle, the required gate charge has to pass all way from the gate driver supply to the transistor gate pin(through the driver output impedance, the external gate resistor, and the internal gate mesh resistance).

On the other hand, the C_{eq} needs to be discharged during turn off process. As a result, the energy charged in the capacitors will be dumped to the ground through turn off circuitry. Equation (4) is used to calculate the gate charge losses:

$$P_{Gate} = V_{GSmax} \cdot Q_{total} \cdot f \quad (4)$$

4. Turn–off Speed Enhancement Circuits:

Designers typically aim to optimize circuit designs to accelerate the MOSFET turn–off process, due to the fact that the optimal MOSFET turn–on time for highest efficiency is related to diode recovery time. Some application notes mistakenly suggest that if a transistor turns on faster than the parallel diode on the opposite device can turn off, it would cause shoot–through, leading to excessive current passing through both

devices. However, the actual reason for slowing down the transistor's turn-on time is different. In the case of an inductive load, during the dead-time (when both transistors are off), one of the transistors' parallel diodes will conduct, depending on the direction of the load current. For clarity, let's assume the load current direction is as depicted in Fig. 5.

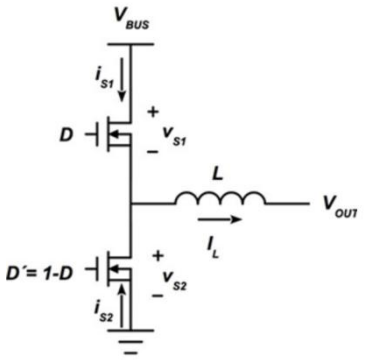

Fig.5. half bridge configuration in which each transistors contains a parallel diode

During the dead-time, the parallel diode of the lower transistor conducts the load current. Once the dead-time ends and the higher transistor begins to turn on, the load current is shared between the higher transistor and the parallel diode of the lower transistor. The reverse recovery of the parallel diode causes an overshoot in the current flowing through the higher transistor, as shown in Fig. 6.

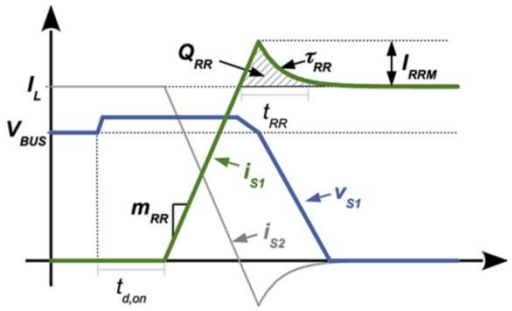

Fig.6. ***Control switch S1 turn-on waveforms showing dead-time and reverse recovery. Current waveform of rectifier S2 show for reference***

The value of reverse recover current (I_{RRM}) depends on several factors, including the load current (I_L), the bus voltage (V_{BUS}) and the rate at which the current in the lower transistor's parallel diode decreases. This rate of current decay is, in turn, dependent on the turn-on speed of the higher transistor. The faster the higher transistor turns on, the quicker the current in the lower diode declines, resulting in a higher I_{RRM}.

Followings are few important points to consider:

- If the higher transistor switches ON too rapidly, the peak reverse recovery current of the lower parallel diode will rise too rapidly, the peak reverse recovery current rating will be exceeded, and the device may possibly be destroyed.

- Higher I_{RRM} means higher losses as well as higher Electromagnetic interference (EMI).

solution: the peak reverse recovery current of the rectifier can be reduced by slowing down the rate of change of current during the commutation process. The rate of change of current can be controlled by purposefully slowing down the rate of rise of the gate driving pulse. Using this technique, the peak current can be reduced to almost any desired extent, at the expense of prolonging the high dissipation switching period.

As a result, during turn on, the fastest switching action is determined by the reverse recovery characteristic of the diode, not by the strength of the gate drive circuit. In an optimum design, the gate drive speed at turn–on is matched to the diode switching characteristic.

The situation differs significantly during turn–off. In theory, the turn–off speed of the MOSFET is influenced solely by the gate drive circuit. A turn–off circuit with higher current capability can discharge the input capacitors more rapidly, resulting in shorter switching times and reduced switching losses. Achieving a higher discharge current can be accomplished through a MOSFET driver with a lower output impedance and/or applying a negative turn–off voltage at the drive output in the case of a N–channel device. However, while faster switching can lower switching losses, the increased turn–off di/dt and dv/dt can induce more ringing in the waveforms. This must be taken into account when selecting the appropriate voltage rating and electromagnetic interference (EMI) containment for the power device.

In some scenarios, it is advantageous to have a **slow turn–on and a fast turn off**. To achieve this, any of following solutions can be employed.

4.1. Turn off diode:

The simplest technique to improve turn–off time is the use of an anti–parallel diode, as illustrated in Figure 7.

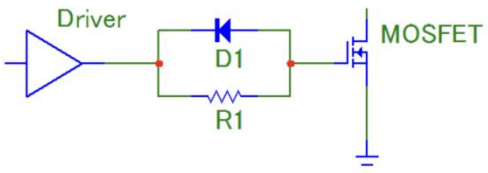

Fig.7. turn off diode to enhance turn off time

In this circuit, R_1 is the parameter to adjust the MOSFET turn–on speed. For larger R1 resistors, the gate current is limited, leading to an increase in turn–on time. Conversely, with smaller R1 resistors, the circuit may experience oscillations, as discussed in Section 4. Therefore, the value of R_1 should be selected analytically to achieve an optimized design for turn–on performance. This careful selection ensures a balance between

switching speed and efficiency, minimizing losses while preventing issues like excessive ringing or cross-conduction (due to diode slow turn-off as discussed in section 3). During turn-off, the anti-parallel diode (D1) bypasses the resistor, allowing the gate current to flow through the diode. D_1 conducts only when the gate current is higher than $\frac{V_{D,FWD}}{R_1}$, otherwise the sink current during off process, will go through the R_1 resistor.

4.2. PNP Turn-off Circuit:

The most common configuration for fast turn-off is the local PNP turn-off circuit, as illustrated in Figure 8. In this setup, the resistor R_{GATE} is used to adjust the turn-on speed, while the diode D_{ON} provides a dedicated path for the turn-on current, ensuring efficient switching control.

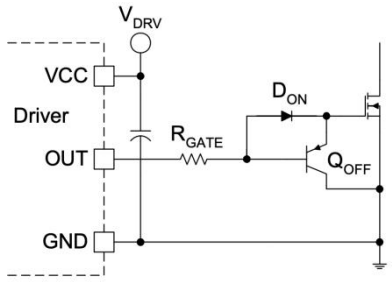

Fig.8. PNP turn-off circuit [1]

The key advantage of this solution is that it confines the high peak discharge current of the MOSFET's input capacitance within the smallest possible loop, specifically between the gate-source of the MOSFET and the collector-emitter of the BJT. This minimizes parasitic inductance, reduces ringing and improves switching efficiency during the turn-off process.

4.3. NMOS Turn-off Circuit:

An enhanced implementation of fast turn-off principle, with a reduced component count, is shown in Figure 9. This design utilizes a dual driver to supply the inverted PWM signal to a small N-channel discharge transistor. This configuration simplifies the circuit while maintaining fast and efficient discharge of the MOSFET's gate capacitance during turn-off, improving overall performance and reducing switching losses.

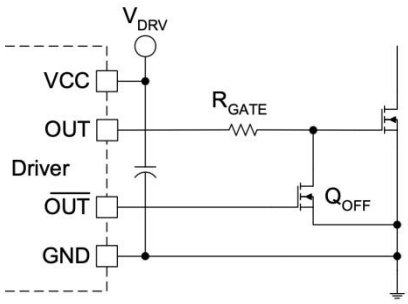

Figure.9. Improved N-Channel MOSFET-Based Turn-off Circuit [1]

This circuit enables very fast switching and ensures the complete discharge of the MOSFET gate to 0V. As before, R_{GATE} is used to adjust the turn-on speed, but it also serves to prevent shoot-through currents between the two outputs of the driver in case of imperfect signal timing. Another important fact to consider is that the C_{OSS} capacitance of Q_{OFF} is connected in parallel to the CISS capacitance of the main power MOSFET. This increases the effective "Total Gate Charge" the driver has to provide. Also to consider, the gate of the main MOSFET is floating before the outputs of the driver IC becomes intelligent during power up.

5. Parasitic Oscillation:

No matter what precautions we take, some level of stray inductance will always exist in the gate driver, as well as in gate and source circuitry. As a result, the input capacitance (C_{ISS}), gate resistor (R_G), and stray inductance (L) form a resonant circuit.

✧ **Source Inductance**: The source inductance (L_S) has the most significant impact on switching performance. In a typical circuit, there are three primary sources of parasitic source inductance:

- The source bond wire, which is neatly integrated into the MOSFET package.
- The printed circuit board (PCB) wiring inductance between the source lead and the common ground.
- Current sense resistors in series with the source.

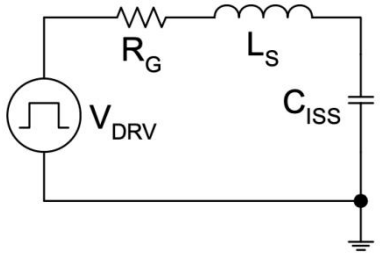

Fig.10. Gate-Drive Resonant Circuit Components

The following cases illustrate the effect of source inductor during the switching procedure:

1. **Extending the duration the tun on/off delay**: The gate current increases very rapidly at the turn–on and turn–off delays (step 1) as shown in here. The source inductance slows it down depending on the inductor's value. As a result, the time required to charge or discharge the MOSFET's input capacitance is extended, significantly affecting the turn–on and turn–off delays.

2. **Creating Resonant Circuit**: Additionally, the source inductor and the C_{ISS} capacitor create a resonant circuit, as depicted in Figure 10. This resonance can lead to oscillations that impact switching performance. The resonant circuit is triggered by the steep edges of the gate drive voltage waveform, which is the primary cause of the oscillatory spikes commonly seen in gate drive circuits. A high–Q resonance between the C_{ISS} capacitor and the source inductance (L_S) can be mitigated by introducing series resistive components into the loop. These include the driver output impedance, the external gate resistor, and the internal gate mesh resistor, which help dampen the resonance and reduce the oscillations.

$$Q = \frac{\sqrt{Ls}}{\sqrt{Ciss.R}} \quad (5)$$

Setting Q=0.5, $R_{G,opt}$ can be as follows:

$$R_{G,opt} = \frac{2x\sqrt{Ls}}{\sqrt{Ciss}} - (R_{DRV} - R_{G,I}) \quad (6)$$

The only user adjustable value, $R_{G,opt}$, can be calculated for optimum performance shown in Equation 6. Smaller resistor values will result an overshoot in the gate drive voltage waveform, but also result in faster turn–on speed. Higher resistor values will under damp the oscillation and extend the switching times without offering any benefit for the gate drive design.

3. **Lowering the $\frac{di}{dt}$ of drain current**: The source inductance introduces a negative feedback effect whenever the drain current of the device changes rapidly. This effect is observed during the second time interval of the turn–on process and the third time interval of the turn–off process. During these periods, the gate voltage is between V_{TH} and $V_{GS,Miller}$, and the gate current is determined by the voltage across the drive impedance, $V_{GS,MAX} - V_{GS}$. To increase the drain current quickly, a significant voltage must be applied across the source inductance ($V_L = \frac{Ldi}{dt}$). This voltage reduces the available voltage across the drive impedance, which in turn slows the rate of change of the gate drive voltage and results in a lower $\frac{di}{dt}$ of the drain current. Consequently, the lower $\frac{di}{dt}$

requires less voltage across the source inductance. This interplay establishes a delicate balance between the gate current and the drain $\frac{di}{dt}$ through the negative feedback effect of the source inductance.

Drain Inductance: The other parasitic inductance in the switching network is the drain inductance, which consists of several components: the packaging inductance within the transistor package, the inductances associated with interconnections, and the leakage inductance of transformers in isolated power supplies.

During turn–on, the drain inductance limits the $\frac{di}{dt}$ of the drain current and reduces the drain–to–source voltage across the device by a factor of $\frac{L_D.di}{dt}$. This can significantly reduce turn–on switching losses. While higher values of L_D appear advantageous during turn–on, they pose significant challenges during turn–off. For rapid reduction of the drain current during turn–off, a voltage in the opposite direction relative to turn–on must be applied across L_D. This results in a voltage overshoot above the theoretical $V_{DS,off}$ level, leading to an increase in turn–off switching losses. The voltage surge across the drain and the source is superimposed on the V_{GS} voltage via the gate–drain capacitance Cgd of the MOSFET and might cause ringing of the gate voltage. A large ringing voltage superimposed on the gate voltage might cause the MOSFET to turn on and off repeatedly, leading to oscillation of the MOSFET as shown in Figure 11.

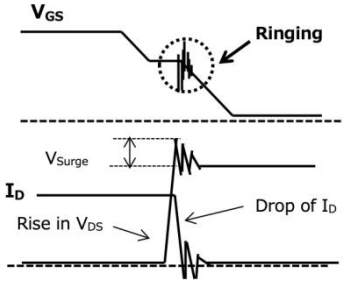

Fig.11. Effect of drain leakage inductance on turn–off waveforms [2]

6. High Side Gate Driver:

In applications using a half–bridge configuration, the gate driver for the upper switch must apply voltage to the gate relative to the upper switch's source pin (which is also the drain pin of the lower switch). Since the voltage at this pin is constantly changing and floating, specialized circuitry is required to effectively drive the upper switch. In another words, driving a high–side MOSFET (or other high–side switches) requires a voltage higher than the supply voltage to turn the switch on fully.The following circuits are suggested for this purpose:

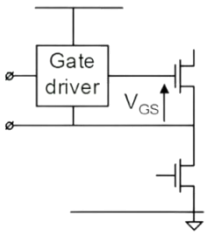

Fig.12. high-side gate driver

6.1. Transformer:

By applying straightly pulses to primary, and considering N_2/N_1 ration, secondary can provide required V_{GS} voltage for the upper switch. However, there are few concerns to consider while using this method:

6.1.1. zero average:

First concern is, pulses on the primary side should have zero average, otherwise the transformer will be saturated. To take care of that, a capacitor is used on the primary side. Fig.13 shows the capacitor effect. However, using this method, the DC shift depends on the pulse shape. At wide duty cycles the circuit of Figure 13 does not provide adequate gate drive voltage. The coupling capacitor voltage increases proportionally to the duty ratio. Accordingly, the negative bias during off-time increases as well and the turn-on voltage decreases.

Fig.13. coupling capacitor to provide the reset voltage for the magnetizing inductance

A better solution is shown in Fig.14. by applying the pulse to the transistor, it will transfer the pulse to the secondary side considering n_1/n_2 ratio. By turning-off the transistor, the auxiliary winding will take care of resetting the magnetization of the transformer, and it will apply a negative voltage at n_1 winding, which will help to turn-off the MOSFET faster.

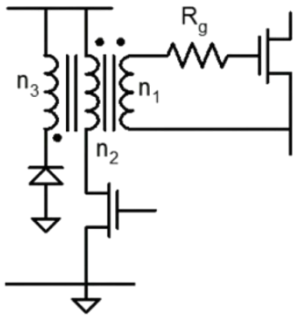

Fig.14. forward converter

Another way to improve transformer saturation problem, is DC restorer which is shown in Fig.15. It shows a commonly used technique to restore the original voltage levels of the gate drive pulse. Here, a second coupling capacitor (C_{C2}) and a simple diode clamp (D_{C2}) are used to restore the original gate drive amplitude on the secondary side of the transformer. If a larger negative bias is desired during the off time of the main switch, a zener diode can be added in series with the diode[1].

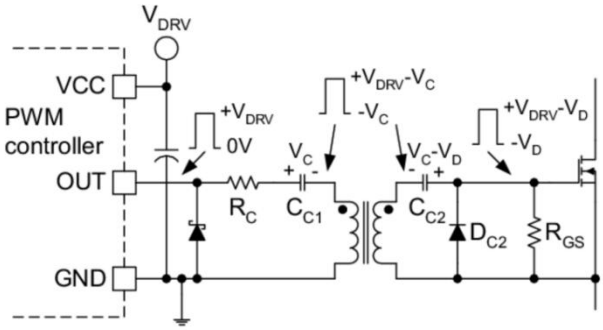

Fig.15. transformer leakage inductance [1]

A more advanced circuit is shown in Fig. 16. In this configuration, C_2 and D_2 form the restorer circuitry, while the push–pull driver is built using Q_1 and Q_2 BJTs. C_3 serves as the power supply for the push–pull driver, eliminating the need for a floating power source. This capacitor is charged through diode D_1 during the positive pulse.

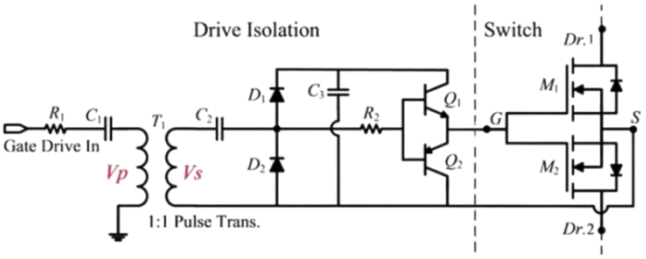

Fig.16. DC restorer driver

6.1.2. **Leakage Inductance:**

Ideally, a transformer does not store energy, with no exceptions. However, in real transformers, small amounts of energy are stored in the nonmagnetic spaces. This energy storage is reflected in the leakage and magnetizing inductance which is the

second concern of using transformer for high-side gate drive circuity. In power transformers, minimizing leakage inductance is crucial to reduce energy storage and ensure high efficiency. While gate drive transformers handle very low average power, they must supply high peak currents during turn-on and turn-off. To prevent delays in the gate drive path, keeping leakage inductance low remains essential. Transformer leakage inductance cause oscillation on the output voltage.

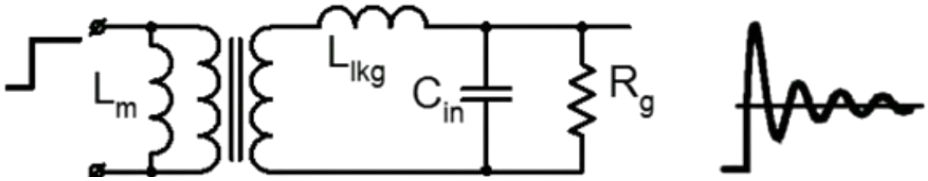

Fig.17. transformer leakage inductance

6.2. Optical:

One simpler solution compared to using transformer, is using optocoupler. In this case, we need to make sure the optocoupler is fast enough to not to effect rising and falling time. A driver is needed at the next stage of the circuit, to amplify the current for the gate pin. In this method, a floating power supply is need.

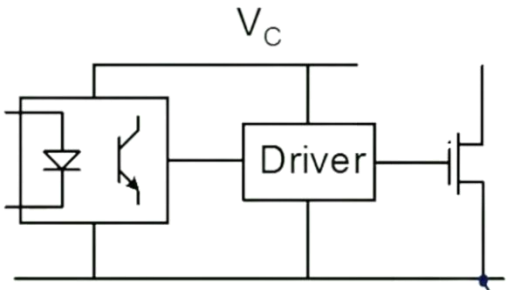

Fig.18. Optical solution for high side driver

6.3. Bootstrap:

A common approach that uses a bootstrap capacitor to provide a floating power supply to the upper gate driver. Fig.19 shows the bootstrap circuit to drive upper MOSFET in a leg. In the meanwhile lower switch is on, the source pin of upper switch is near ground (low R_{DS-on} on lower switch), so During this time, the bootstrap diode allows current to flow and charge the bootstrap capacitor from the supply voltage (typically 12V or 15V).

When the low-side MOSFET turns off and the high-side MOSFET needs to be switched on, the charge stored in the bootstrap capacitor (C_{BST}) is used to provide a higher voltage relative to the source of the high-side MOSFET, turning it on fully. The

bootstrap capacitor provides the gate drive voltage to keep the high-side MOSFET turned on until the next cycle when the capacitor is recharged.

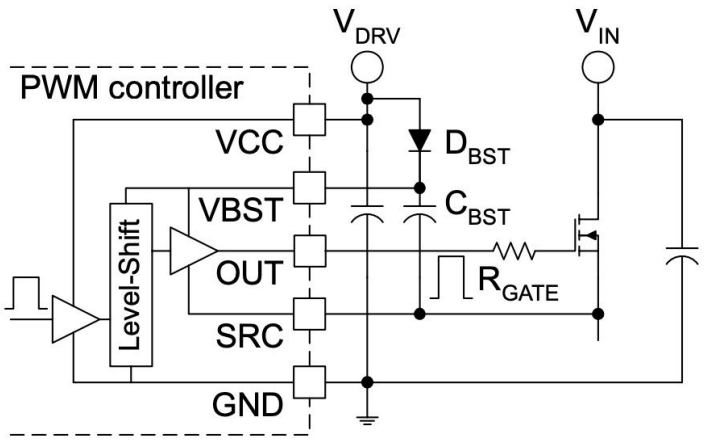

Fig.19. Bootstrap circuit for high-side driver

7. Ground-Referenced Gate Driver:

Ground-referenced gate drivers are primarily used in circuits where the low-side switch is referenced to ground, and to drive the low-side MOSFET or IGBT.

7.1.1. PWM Direct Drive:

In power supply applications, the simplest way of driving the gate of the main switching transistor is to utilize the gate drive output of the PWM controller as shown in Figure 20.

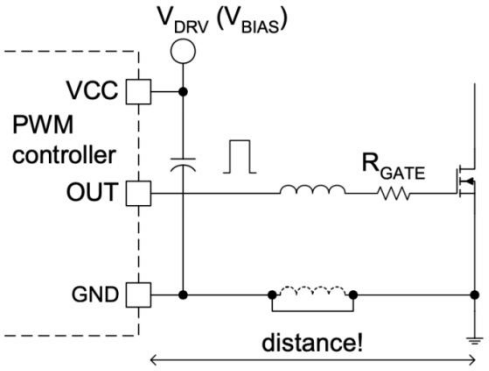

Fig.20. Direct gate driver circuit

The most challenging aspect of direct gate drives is optimizing the circuit layout. As shown in Figure 20, significant distances between the PWM controller and the MOSFET can introduce parasitic inductance from the loop formed by the gate drive and

ground return traces. This inductance can slow down switching speeds and cause ringing in the gate drive waveform. Even with a ground plane, inductance cannot be completely eliminated, as the ground plane only provides a low-inductance path for ground return current. To minimize this inductance, using wider PCB traces for the gate drive connection is advantageous.

Another challenge with direct gate drive is the limited drive current capability of PWM controllers. Few integrated circuits can handle peak gate drive currents above 1 A, which restricts the size of MOSFETs that can be driven effectively by the controller. Power dissipation within the controller also limits the maximum MOSFET die size when using direct gate drive. An external gate resistor can help mitigate this issue.

When direct gate drive is necessary for space or cost reasons, careful consideration is needed for bypassing the controller. High current spikes required to drive the MOSFET gate can interfere with the sensitive analog circuitry inside the PWM controller. As the MOSFET die size increases, so does the required gate charge, necessitating a more scientific approach to selecting the appropriate bypass capacitor rather than just using a standard 0.1 μF or 1 μF capacitor.

Additionally, for gate drive ICs with a bipolar output stage, it is crucial to provide protection against reverse currents. As illustrated in Figure 21, integrated bipolar drivers use npn transistors due to their efficient area utilization and superior performance.

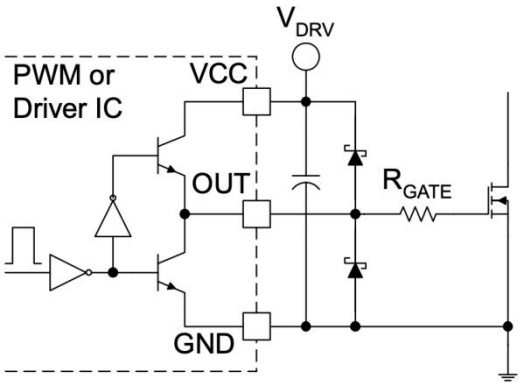

Fig.21. Gate drive with integrated bipolar transistor

NPN transistors can only handle current in one direction. Specifically, the high-side NPN transistor can source current but cannot sink it, while the low-side NPN transistor can only sink current. During MOSFET turn-on and turn-off, unavoidable oscillations between the source inductor and the input capacitor require that current flow in both directions at the driver's output. To accommodate reverse currents, low forward voltage drop Schottky diodes are typically used to protect the driver outputs.

These diodes should be placed as close as possible to the output pin and the driver's bypass capacitor.

It is also crucial to note that these diodes only protect the driver from reverse currents, and they do not address excessive ringing of the gate-to-source voltage. In systems with direct drive, where the control IC may be located far from the gate-source terminals of the MOSFET, additional measures may be needed to manage voltage ringing and ensure stable operation.

7.1.2. **Bipolar Totem-Pole Drive:**

To address the drawbacks of PWM direct drive and achieve faster switching, one effective method is to introduce a current amplifier between the PWM controller and the MOSFET. By doing this, the current amplifier can supply substantial current to the MOSFET gate, enabling faster switching speeds. This approach helps to overcome the limitations of the PWM controller's drive capability and enhances the performance of the gate drive. To achieve this, using BJTs can be beneficial due to their fast switching capabilities in linear mode, high pulse current capability, high current density, small size, and cost-effectiveness.

One of the most popular and cost effective drive circuit for driving MOSFETs is a bipolar, non-inverting totem-pole driver as shown in Figure 22. The circuit typically consists of two BJTs: an NPN transistor placed at the high side and a PNP transistor positioned at the low side. This arrangement forms a complementary push-pull configuration that efficiently drives the MOSFET gates with high current capability and fast switching speeds.

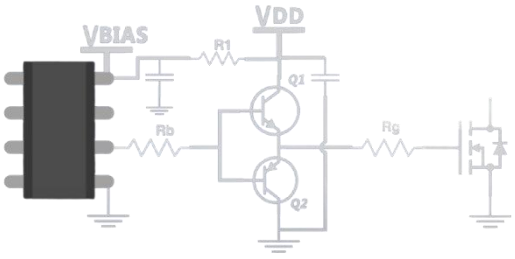

Fig.22. Bipolar Based Totem-Pole MOSFET Driver

Like all external drivers, this circuit handles the current spikes and power losses making the operating conditions for the PWM controller more favorable. Of course, they should be placed right next to the power MOSFET they are driving. That way the high current transients of driving the gate are localized in a very small loop area, reducing the value of parasitic inductances. Even though the driver is built from discrete components, it needs its own bypass capacitor placed across the collectors of the upper npn and the lower pnp transistors. Ideally there is a smoothing resistor (R_1) or inductor between the

bypass capacitor of the driver and the bypass capacitor of the PWM controller for increased noise immunity. The R_g resistor of Figure 22 is optional and R_b can be sized to provide the required gate impedance based on the large signal beta of the driver transistors.

An interesting property of the bipolar totem–pole driver is that the two base–emitter junctions protect each other against reverse breakdown. Furthermore, assuming that the loop area is really small and R_g is negligible, they can clamp the gate voltage between $V_{BIAS}+V_{BE}$ and $GND-V_{BE}$ using the base–emitter diodes of the transistors. Another benefit of this solution, based on the same clamp mechanism, is that the npn–pnp totem–pole driver does not require any Schottky diode for reverse current protection.

7.1.3. **MOSFET Totem–Pole Drive:**

To achieve higher speed and faster conversion frequencies, the totem–pole circuitry can be implemented with MOSFETs instead of BJTs. The MOSFET equivalent of the bipolar totem–pole driver is illustrated in Fig. 23. All the benefits mentioned about the bipolar totem–pole driver are equally applicable to this implementation.

However, there are some notable drawbacks compared to the bipolar version:

1. **Inversion Requirement:** The MOSFET totem–pole driver is an inverting driver, so the PWM output signal must be inverted to match the desired logic.
2. **Cost:** Suitable MOSFETs are generally more expensive than their bipolar counterparts, which can increase the overall cost of the circuit.
3. **Shoot–Through Current:** MOSFETs can experience significant shoot–through current when the gate voltages are transitioning. This issue arises because both MOSFETs in the totem–pole arrangement can momentarily be on at the same time, leading to a direct short between the supply voltage and ground.

   Solution: This problem can be mitigated with additional logic or timing components, which is commonly employed in integrated circuit (IC) implementations to manage timing and prevent shoot–through conditions.

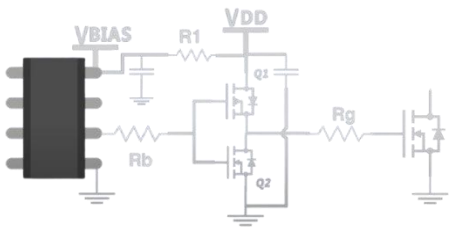

Fig.23. MOSFET Based Totem–Pole MOSFET Driver

8. Open Points:

8.1. Resistor Across Gate-Source pins:

The gate-source parallel resistor (R_G) is to provide a path to ground. Since this resistor (R_G) and series gate resistor (R_1) in the circuit forms a voltage divider, if the R_G resistor was a lower value, then the value of voltage across gate-source pins (Vgs) would be affected during both turn-on and turn-off intervals. A high resistance (often in the range of 100kΩ to 1MΩ) providing a ground path while keeps the signal current very low while, so that it does not significantly affect the switching speed or the performance of the MOSFET.

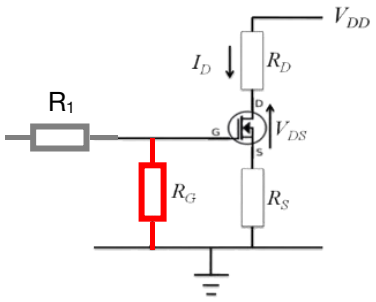

Fig.24. Gate-Source large resistance

All reasons of using this resistor are summarized as follows:

8.1.1. Gate Discharge Path:

Once the Cgs capacitor is charged, it can hold the gate voltage for a long time. The high-value resistor provides a discharge path for this gate charge, ensuring that the gate voltage drops to zero when the driving signal is removed, turning off the MOSFET completely.

8.1.2. Preventing False Turn-On and Stabilizing the Gate Voltage:

a MOSFET is controlled by the voltage (Vgs) applied across gate and source pins. In high-impedance circuits with floating gates, noise or leakage currents can cause the gate voltage to rise unintentionally, turning the MOSFET on when it shouldn't. To prevent this, a high-value resistor is placed between the gate and the source, ensuring the gate is consistently pulled back to a reference potential—often ground (0 V for NMOS or VDD for PMOS)—when the gate control circuit is disconnected or in a high-

impedance state. This helps stabilize the MOSFET in a well-defined state when it's not actively being controlled.

8.1.3. **Leakage Current Handling**:

In some applications, the MOSFET driver may have a small amount of leakage current. The high-value resistor helps to bleed off this leakage current, ensuring that the gate voltage does not rise due to these small currents.

8.2. Zener Diode Across Gate-Source pins:

A Zener diode is often placed across the gate-source pins of a MOSFET to protect it from excessive gate voltage.

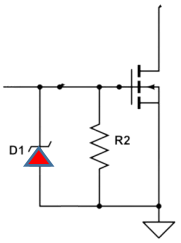

Fig.25. Zener Diode across Gate-Source pins

MOSFET gates are sensitive to high voltages, and exceeding the maximum gate-source voltage rating can permanently damage the MOSFET. The over-voltage situation could be due to high supply voltage of gate driver IC (and consequently applying high voltage across the gate-source pins during the turn-on), or during switching, voltage spikes can occur due to parasitic inductances or other factors in the circuit. In the first case, a Zener diode clamps the the Vgs voltage to a safe level, preventing gate breakdown. So it ensures the MOSFET operates within its recommended voltage range, allowing it to function correctly without overstressing the gate structure. In the later case, a Zener diode helps to absorb these transients, protecting the gate from sudden surges that could exceed the gate oxide breakdown voltage.

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